

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A field effect transistor, comprising:
 - a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;
 - a gate dielectric layer disposed superjacent the bottom portion of the recess, adjacent the substantially vertical sidewalls, and superjacent a portion of a top surface of the substrate;
 - a gate electrode completely overlying the gate dielectric layer; and
 - source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed;
- wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, and wherein the extension extends to approximately a junction of the vertical sidewalls and the bottom portion of the recess a portion of the gate dielectric layer overlaying an innermost portion of the extension.

2. (Previously Presented) The transistor of Claim 1, further comprising a portion of the gate electrode that overlies the innermost portion of the extension.

3. (Previously Presented) The transistor of Claim 2, wherein the gate electrode conforms to a recessed channel.

4. (Currently Amended) A field effect transistor, comprising:
a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;
a gate dielectric layer disposed superjacent the bottom portion of the recess, adjacent the tapered sidewalls, and superjacent a portion of a top surface of the substrate;
a gate electrode completely overlying the gate dielectric layer; and
source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;
wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, and wherein the extension extends to approximately a junction of the tapered sidewalls and the bottom portion of the recess a portion of the gate dielectric layer overlaying an innermost portion of the extension.

5. (Previously Presented) The transistor of Claim 4, wherein a portion of the gate electrode overlies an innermost portion of the extension.
6. (Previously Presented) The transistor of Claim 4, wherein the gate electrode conforms to a recessed channel.
7. (Previously Presented) A field effect transistor, comprising:
 - a substrate having a recess in a surface thereof, the recess having a curvilinear shape;
 - a gate dielectric layer disposed superjacent the curvilinear recess and superjacent a portion of a top surface of the substrate;
 - a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls; and
 - wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension.
8. (Previously Presented) The transistor of Claim 7, wherein the gate electrode conforms to a recessed channel.
9. (Previously Presented) The transistor of Claim 7, wherein the gate electrode conforms to a recessed channel.